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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,636	03/29/2001	Hiroyuki Ikeda	09792909-4795	5712

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ROBERT J. DEPKE
LEWIS T. STEADMAN
TREXLER, BUSHNELL, GLANGLORGI, BLACKSTONE & MARR
105 WEST ADAMS STREET, SUITE 3600
CHICAGO, IL 60603-6299

EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/821,636	IKEDA, HIROYUKI
	Examiner	Art Unit
	Thien F. Tran	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 39-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 39-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 39-41 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kubota et al. (US 5,808,595).

Kubota et al. discloses a display apparatus comprising a plurality of thin film transistors, each of the thin film transistors (Fig. 1a) comprising a semiconductor thin film 12 constituting a channel 12a and having a threshold voltage, and a first gate electrode 16 on one side the semiconductor thin film and a second gate electrode (a conductive electrode 14) on an opposite side of the semiconductor thin film, and further comprising a means for adjusting the threshold voltage by applying a first threshold adjustment voltage (no bias voltage) to the second gate electrode (the conductive electrode 14) when the first gate electrode receives a first control voltage and applying a second threshold adjustment voltage (-20V) to the second gate electrode when the first electrode receives a second control voltage (see col. 13, lines 27-38 and Fig. 4).

Regarding claim 2, Kubota et al. further discloses the semiconductor thin film 12 constituting the channel 12a made of polycrystalline silicon (col. 12, lines 25-27) and has a thickness 100nm (col. 13, lines 20-21). Kubota et al. further discloses some of the thin film transistors being p-channel transistors. It is a known fact that for p-channel

transistors, the channel 12a is doped of n-type impurity which is either phosphorus or arsenic. Therefore, the channel does not contain boron which is a p-type impurity that effectively affects the formation of a depletion layer.

Regarding claim 3, Kubota et al. further disclose n-channel transistors being turned into those of depletion type wherein the film thickness of the semiconductor thin film 12 is set to not more than two times the maximum thickness of the depletion layer (col. 13, lines 14-18). It is a known fact that for n-channel transistors, the channel 12a is doped of p-type impurity which is boron. Therefore, it is inherent that the semiconductor thin film 12 of the n-channel transistors contains an impurity effectively affecting the formation of a depletion layer.

Regarding claims 40 and 41, it is obvious that the voltage Vgs applied to the first gate electrode varies during the operation (0V when the transistor is not selected, off state or –4V to 8 V when the transistor is selected) is different from the threshold adjustment voltage (-20V as solid line shown in Fig. 4) applied to the second gate electrode during voltage application.

Response to Arguments

Applicant's arguments with respect to claims 1-3 and 39-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tt
October 28, 2005

THIEN TRAN
PRIMARY EXAMINER